

FIG. 3

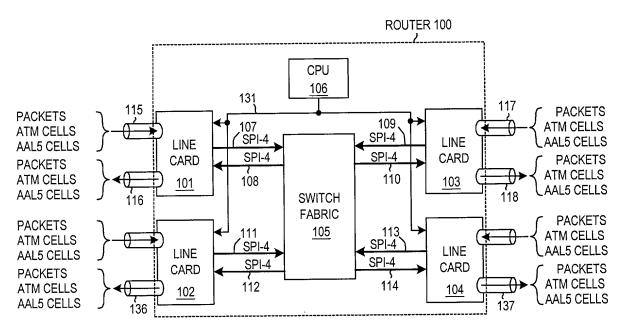


FIG. 4

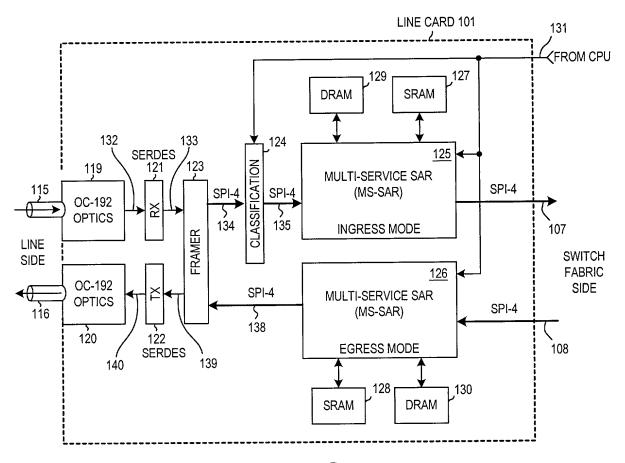


FIG. 5

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SWITCH FABRIC	APPLICATION TYPE	INGRESS APPL TYPE	EGRESS APPL TYPE
CELL	ATM => ATM	0	8
	ATM => MPLS PACKET	1	9
	MPLS PACKET => ATM	2	10
	MPLS PACKET => MPLS PACKET	3	11
	ATM => PACKET	4	14
	PACKET => ATM	6	12
PACKET	AAL5 => PACKET	5	14
	PACKET => AAL5	6	13
	PACKET => PACKET	6	14

APPLICATION TYPES

FIG. 6

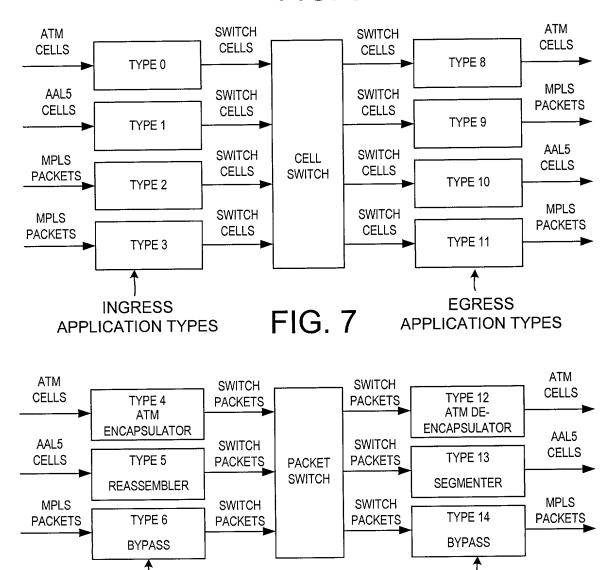


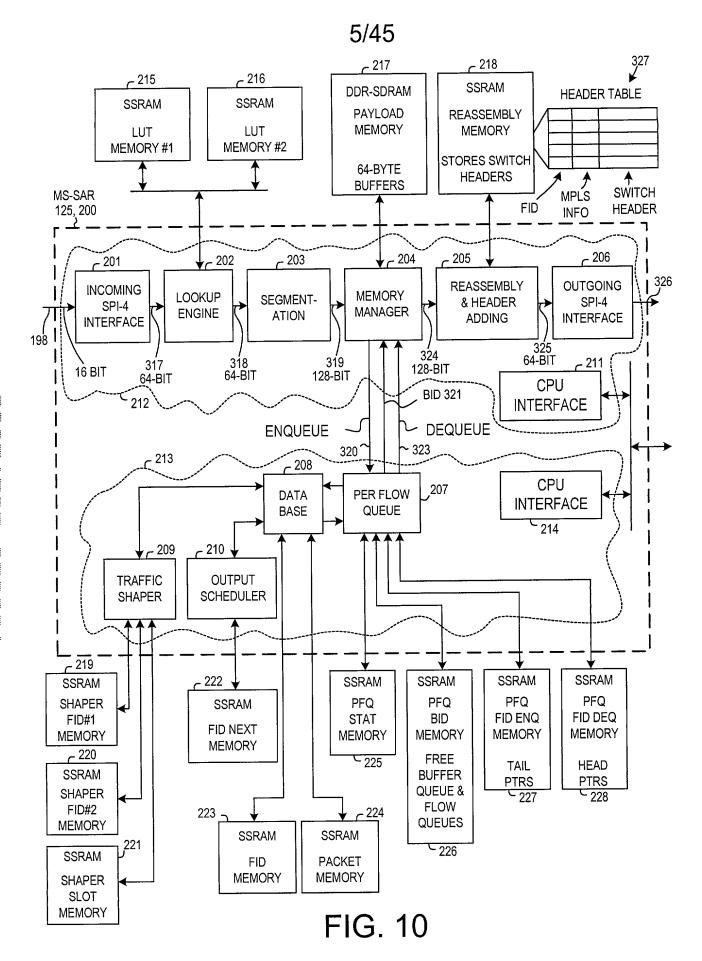
FIG. 8

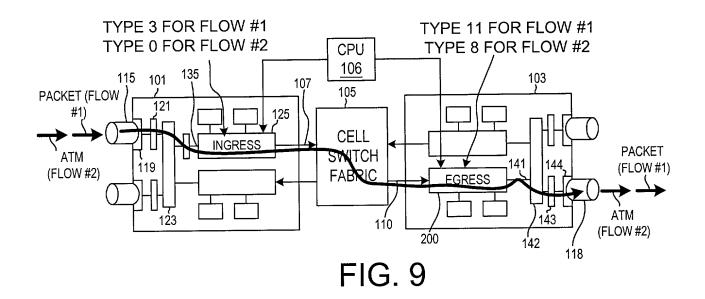
INGRESS

APPLICATION TYPES

EGRESS

APPLICATION TYPES





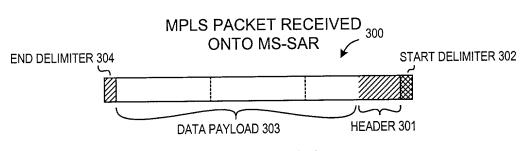


FIG. 11

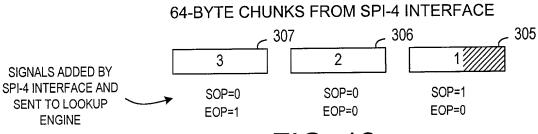


FIG. 12

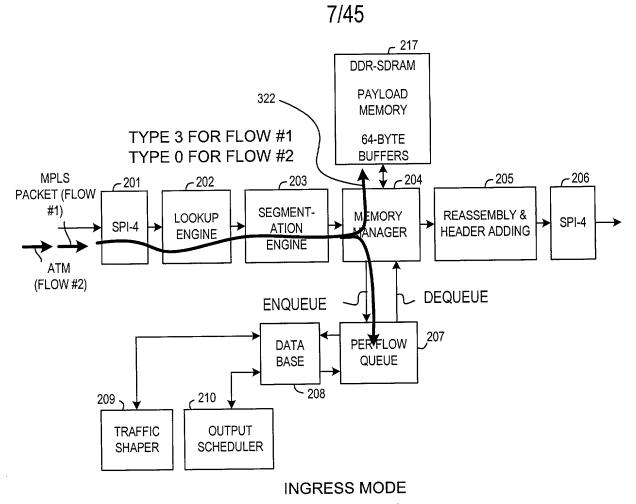


FIG. 13

PORT TABLE IN LOOKUP BLOCK

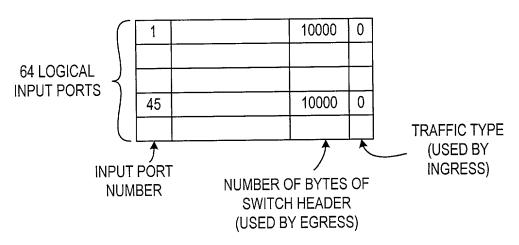
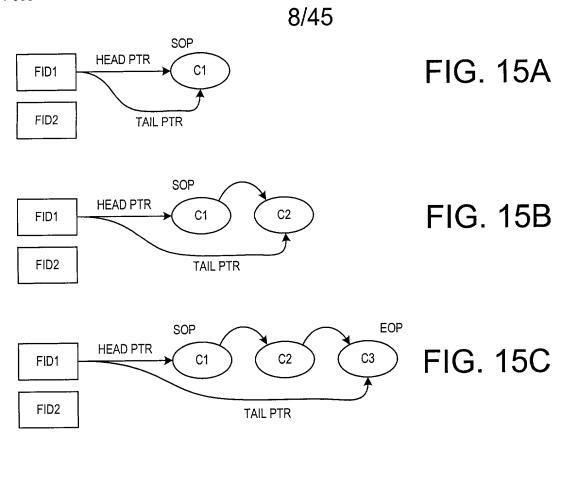
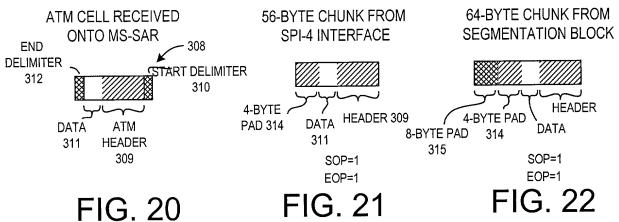


FIG. 14





FID1 HEAD PTR C1 C2 C3

TAIL PTR
FID2 HEAD PTR
C1 C2 C3

TAIL PTR
FIG. 23

NAME	NO BITS	RANGE	WR	DESCRIPTION		
BID HEAD	23	22:0	Н	HEAD POINTER. FIRST BUFFER TO BE ENQUEUED, AND FIRST BUFFER TO BE DEQUEUED. IF NULL, THE QUEUE IS EMPTY.		
HD EOP PKT	1	23	Н	IF SET, THE HEAD BID IS THE EOP.		
HD SOP PKT	1	23	Н	IF SET, THE HEAD BID IS THE SOP.		
HD EFCI	1	25	Н	EFCI BIT.		
CLP	1	26	Н	CLP BIT. CAN BE MODIFIED BY DBS.		
OAM	1	27	Н	OAM BIT.		
SPARE	1	28	Н			
CLASS	3	31:29	Н	CLASS OF FID.		
FID TYPE	4	35:32	Н	APPLICATION TYPE INDICATES THE PROCESSING THAT THE MS-SAR WILL TAKE ON THIS FLOW. WILL BE SENT TO MEMORY MANAGER. TYPE IS WRITTEN WITH THE HEAD POINTER.		

FIG. 16

NAME	NO BITS	RANGE	WR	DESCRIPTION
BID TAIL	23	22:0	Н	TAIL POINTER. LAST BUFFER TO BE ENQUEUED, AND LAST BUFFER TO BE DEQUEUED. IF NULL, THE QUEUE IS EMPTY.
BID PRV PKT TAIL	23	45:23	Н	BID OF PREVIOUS PACKET'S TAIL BID. SAVED ON EOP.
TTL	1	46	Н	WHEN 1, DISCARD AND DEACTIVATE THE FID.
OUTPUT PORT#	7	53:47	S	OUTPUT PORT NUMBER THAT THE FID WILL BE TRANSMITTED ON.
Q SIZE	18	71:54	Н	SIZE OF THE QUEUE IN BIDS. INCREMENTED ON ENQUEUE. DECREMENTED ON EVERY DEQUEUE OPERATION.

FIRST FID ENQUEUE MEMORY LOCATION

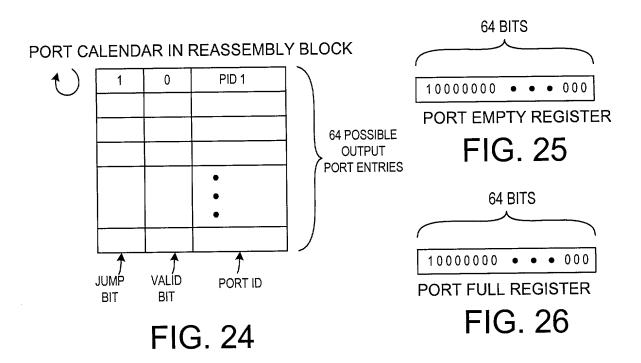
NAME	NO BITS	RANGE	WR	DESCRIPTION
VALID	1	0	S	IF SET, THEN ENQUEUE. IF NOT, THEN SETUP CONNECTION COMMAND AS NEEDED BEFORE ENQUEUE STARTS.
SPARE	8	8:1		
DROP UNTIL SOP	1	9	Н	DROP UNTIL THE NEXT SOP.
SEL DROP COUNT ER	1	10	Н	SEL THE COUNT FOR DROPPING.
SPARE	2	12:11		
CURRENT TAIL PKT CELL CNT	11	23:13	Н	REPRESENTS THE NUMBER OF CELLS IN THE TAIL PACKET THAT IS BEING ENQUEUED.
SPARE	2	25:24		
ENQ NOT DISCARD RED PKT COUNT	16	41:26	Н	THE NUMBER OF NOT DISCARDED PACKETS THAT HAVE ARRIVED SINCE LAST RED DISCARD. IT IS RESET ON THE NEXT RED DISCARD.
SPARE	2	43:42		
AVG	18	61:44	Н	THE AVE SIZE OF THE QUEUE.

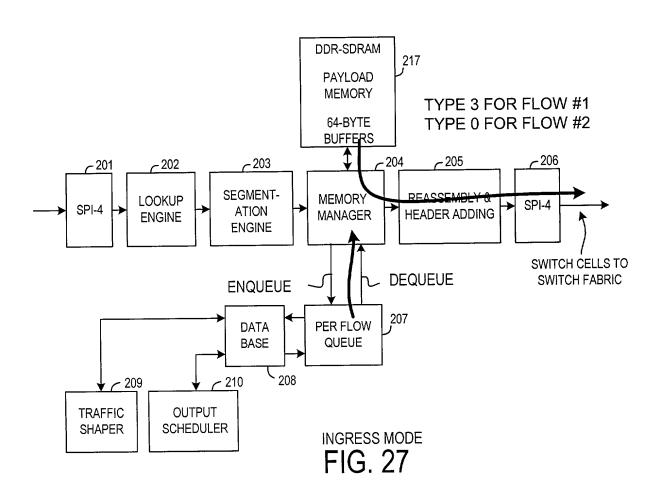
SECOND FID ENQUEUE MEMORY LOCATION

FIG. 18

NAME	NO BITS	RANGE	WR	DESCRIPTION
BID LINK	23	22:0	Н	BID OF THE NEXT BUFFER IN FID QUEUE. ALSO CAN BE A BID LINKED ON THE FREE BUFFER QUEUE.
EOP PKT	1	23	Н	END OF PACKET FOR THIS BID BID. EOP BELONGS TO THE BID LINK.
SOP PKT	1	24	Н	START OF PACKET FOR THE CORRESPONDING BID. SOP BELONGS TO THE BID LINK.
EFCI	1	25	Н	EFCI PASS THROUGH BIT.
OAM	1	26	Н	OAM BIT.
CLP	1	27	Н	CLP
SPARE	8	35:28		

BID MEMORY LOCATION





INDICATES EOP=1

SWITCH HEADER ADDED BY REASSEMBLY BLOCK

64-BYTES

SWITCH CELL #3

64-BYTES

SWITCH CELL #1

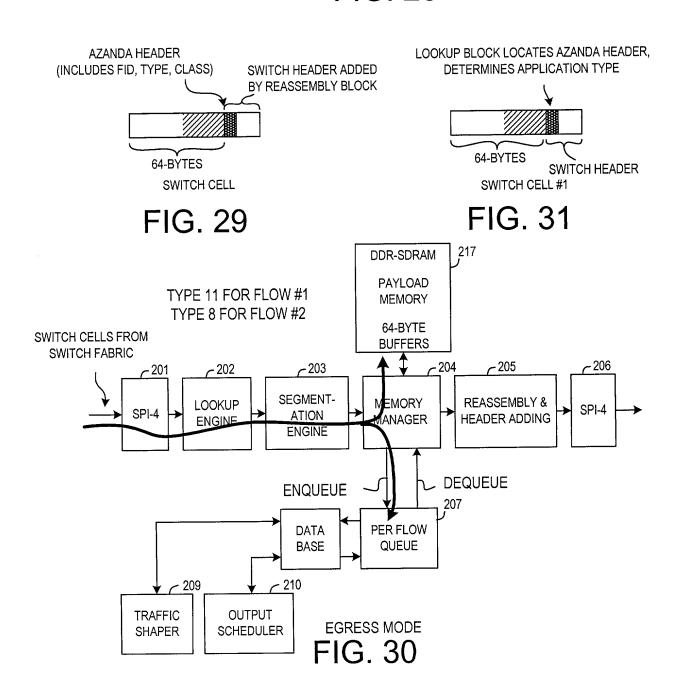
SWITCH CELL #1

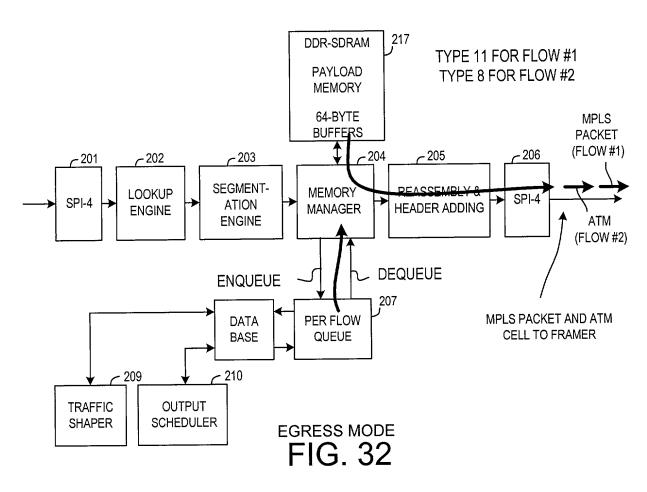
AZANDA HEADER

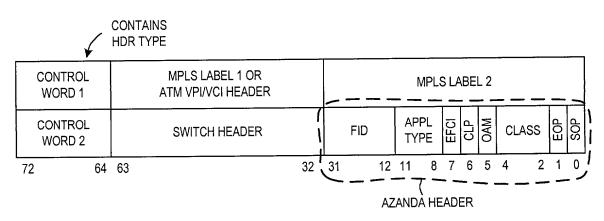
(INCLUDES FID, TYPE, CLASS)

FIG. 28

INDICATES SOP=1







FORMAT OF ONE FID ENTRY IN HEADER TABLE

FIG. 33

64-BYTE CHUNKS FROM REASSEMBLY TO SPI-4

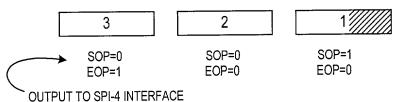


FIG. 34

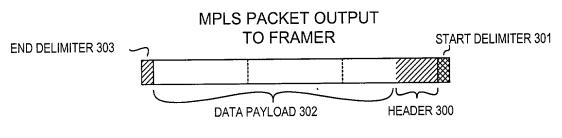
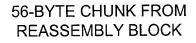


FIG. 35



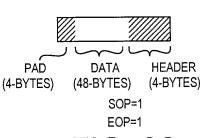


FIG. 36

ATM CELL AS OUTPUT FROM SPI-4 INTERFACE

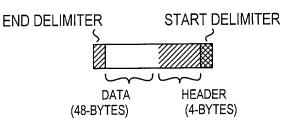


FIG. 37

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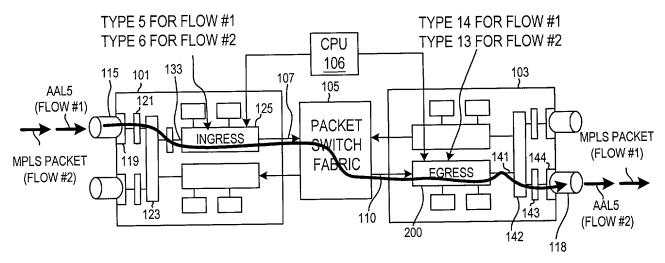
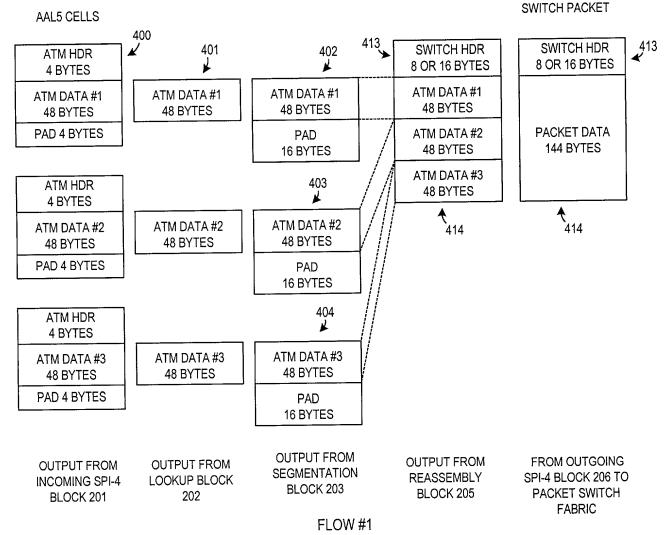
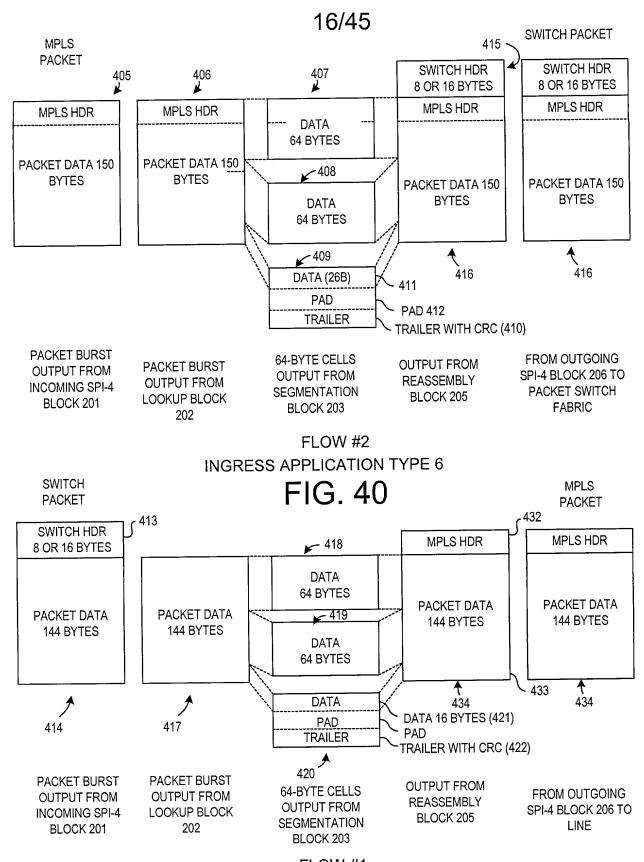


FIG. 38



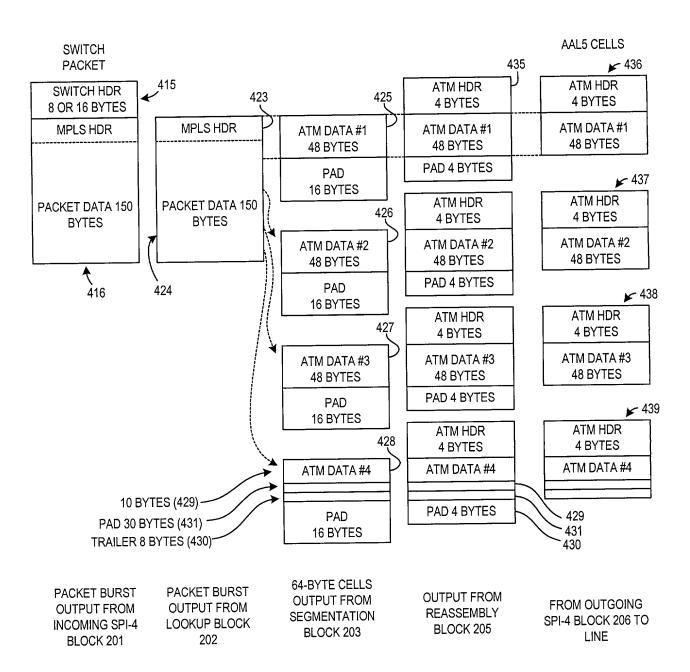
INGRESS APPLICATION TYPE 5

FIG. 39



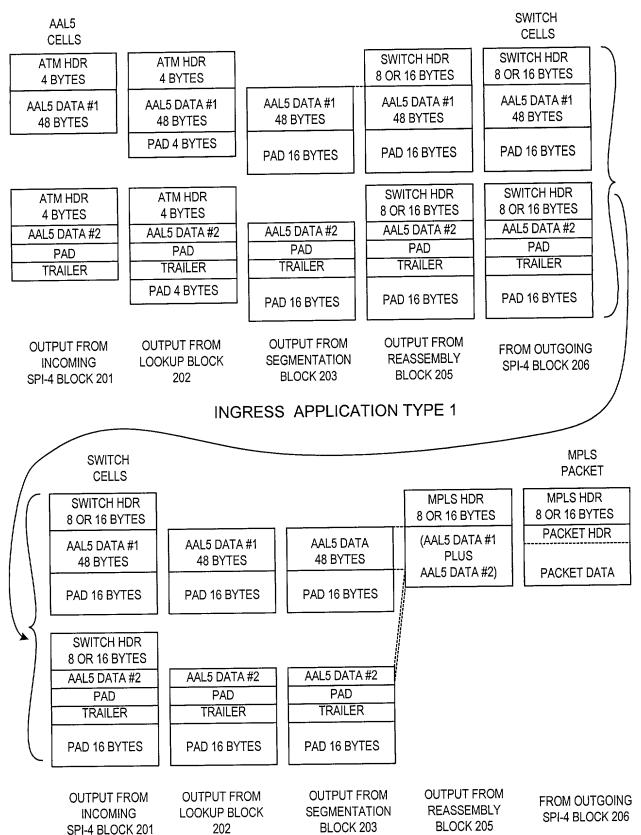
FLOW #1
EGRESS APPLICATION TYPE 14

FIG. 41

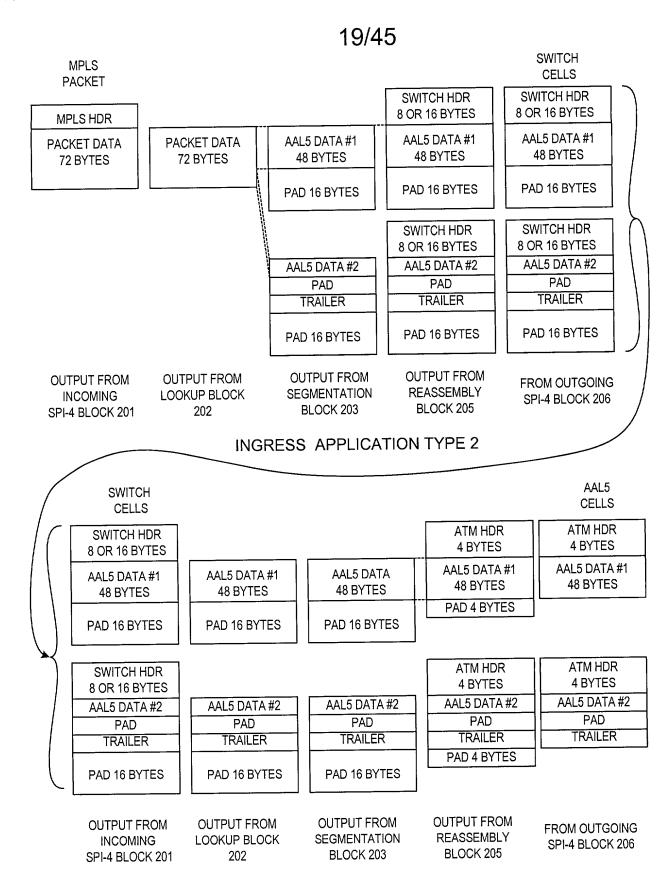


FLOW #2 EGRESS APPLICATION TYPE 13

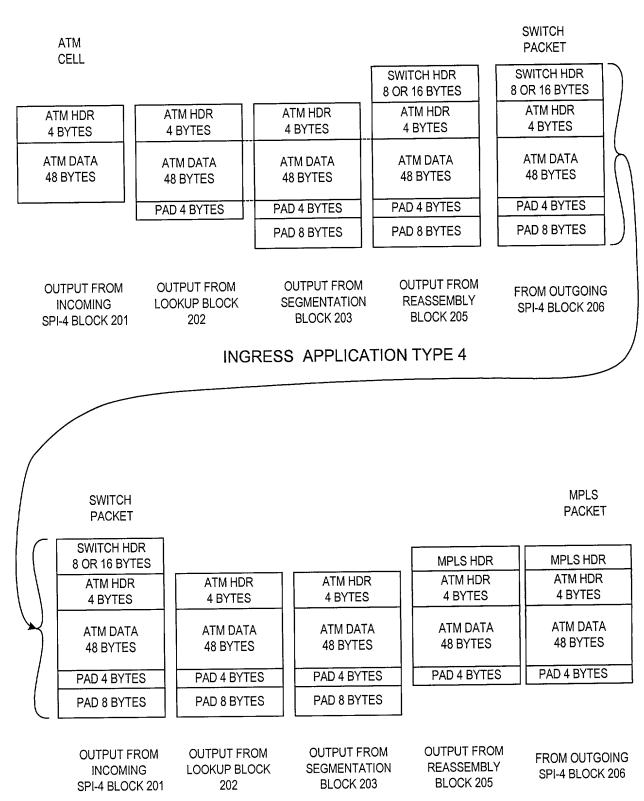
FIG. 42



EGRESS APPLICATION TYPE 9



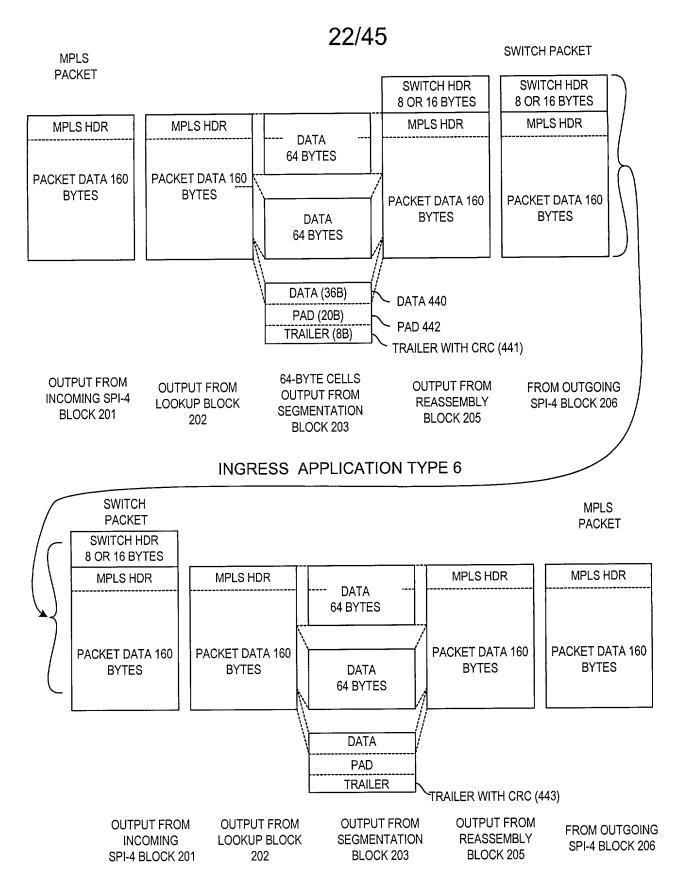
EGRESS APPLICATION TYPE 10 FIG. 44



EGRESS APPLICATION TYPE 14

(A	LS PACKET ATM CELL APSULATED)							CELL EN	PACKET (ATM CAPSULATED) ITCH HDR R 16 BYTES	
MPL	MPLS HDR MPLS HDR MPLS					MF	PLS HDR	М	PLS HDR	
ATI	M HDR	AT	TM HDR		rm HDR	ATM HDR			TM HDR	
4 E	BYTES	4 1	BYTES 4		BYTES	4	4 BYTES		BYTES	\mathcal{A}
1	ATM DATA 48 BYTES		M DATA BYTES	i .	M DATA B BYTES		TM DATA B BYTES	1	ATM DATA 48 BYTES	
L		PAD	4 BYTES	PAD	4 BYTES	PA	0 4 BYTES	PAI	PAD 4 BYTES	
				PAD	8 BYTES					
INC	PUT FROM COMING BLOCK 201	LOOK	UT FROM JP BLOCK 202	SEG	TPUT FROM MENTATION LOCK 203	RE.	IPUT FROM ASSEMBLY LOCK 205		M OUTGOING 4 BLOCK 206	
	SWITCH PACK			ESS	APPLICAT	TON T	YPE 6			/
	SWITCH H 8 OR 16 BY								ATM CELL	
	MPLS HE									
	ATM HD		ATM HD	R	ATM HD	R	ATM HDR		ATM HDR	
>				3	4 BYTES		4 BYTES		4 BYTES	
	ATM DATA 48 BYTES 48 BYTES		S	48 BYTES		S 48 BYTES		ATM DATA 48 BYTES		
	PAD 4 BY	TES	PAD 4 BY1	ES	PAD 4 BY			ES		
					PAD 8 BY	IES				
	OUTPUT FROM OUTPUT FROM INCOMING LOOKUP BLOCK SPI-4 BLOCK 201 202				OUTPUT FI SEGMENTA BLOCK 2	TION	OUTPUT F REASSEM BLOCK 2	IBLY	FROM OUTGO SPI-4 BLOCK	

EGRESS APPLICATION TYPE 12 (ATM DE-ENCAPSULATION)



EGRESS APPLICATION TYPE 14

FIG. 47

D

u

FIG. 48

PACKET OUT OF DISTRIBUTION CHIP

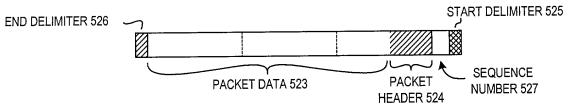
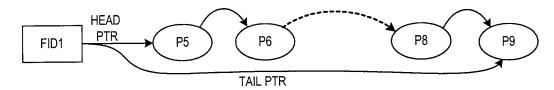
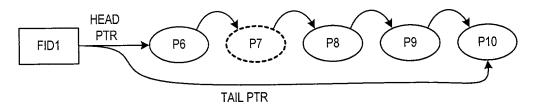


FIG. 49



PACKET QUEUE

FIG. 50



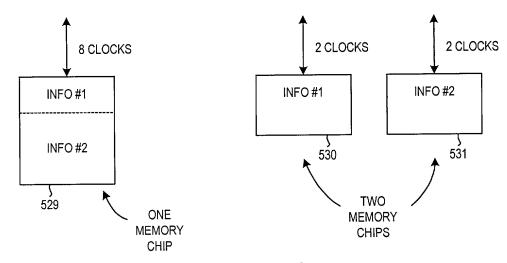


FIG. 52

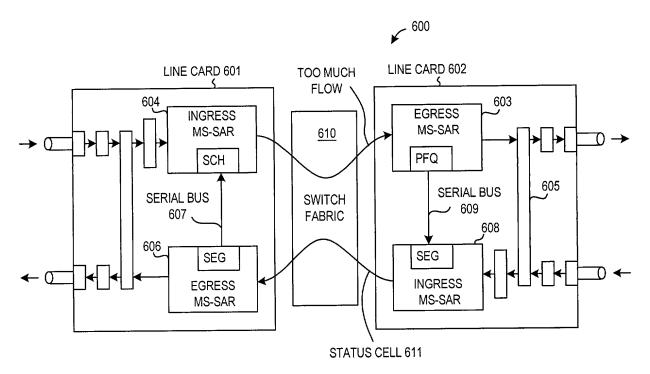
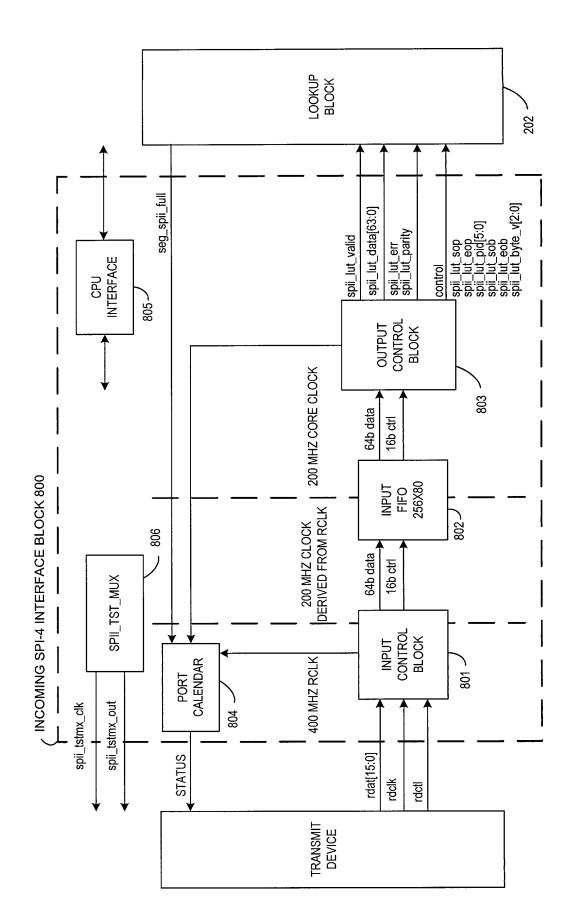
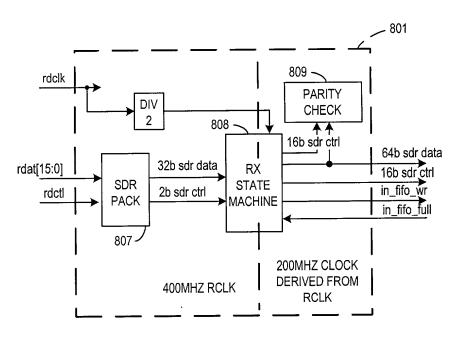


FIG. 53



INCOMING SPI-4 INTERFACE BLOCK

FIG. 54



INPUT CONTROL BLOCK

FIG. 55

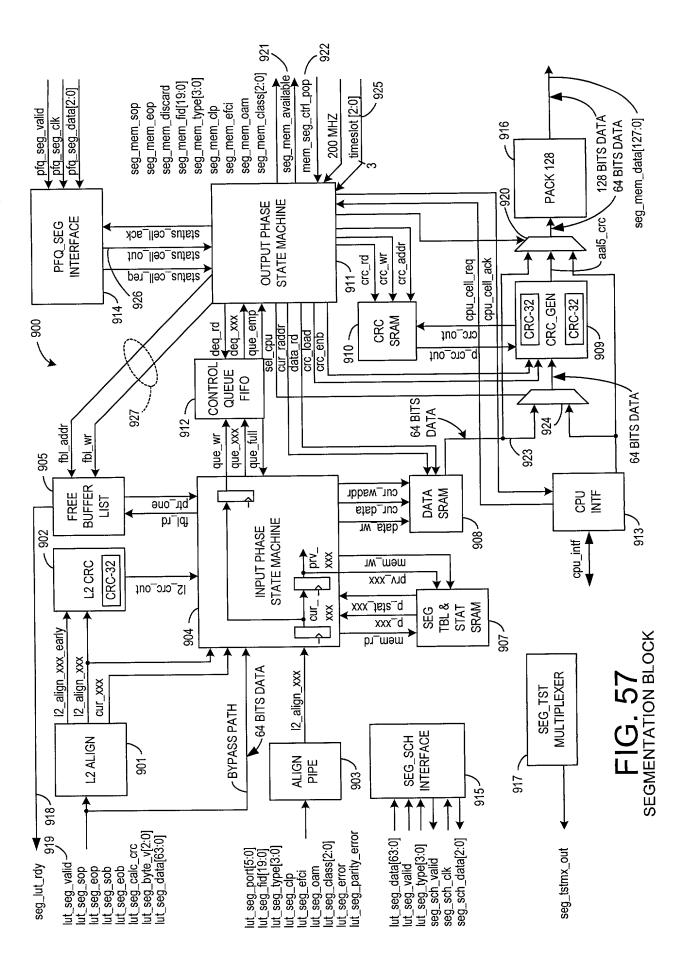
- 803 815 ~ FREE BUFFER LIST output_fifo_full 812 -810 spii_lut_data [63:0] DATA spii_lut_sop FIFO spii_lut_eop spii_lut_sob 813 in_fifo_out spii_lut_eob PER OUTPUT spii_lut_pid[5:0] CONTROL in_fifo_empty **PORT** CONTROL spii_lut_byte_v[2:0] spii_lut_err **FIFO** CONTROL in_fifo_rd spii _lut_parity spii_lut_valid 814 /

OUTPUT CONTROL BLOCK

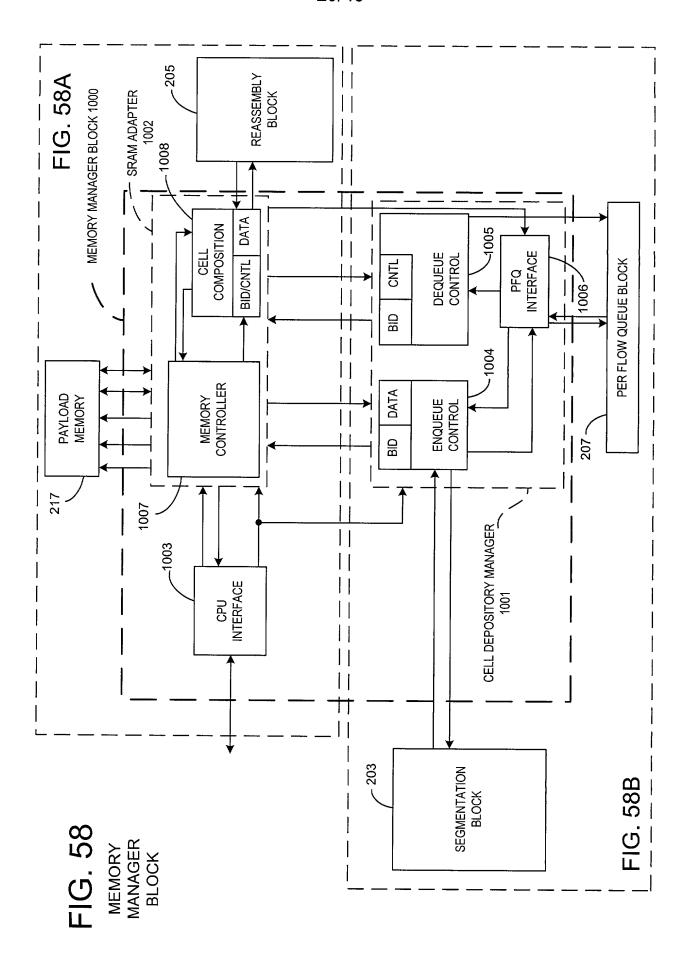
811

SPI TABLE

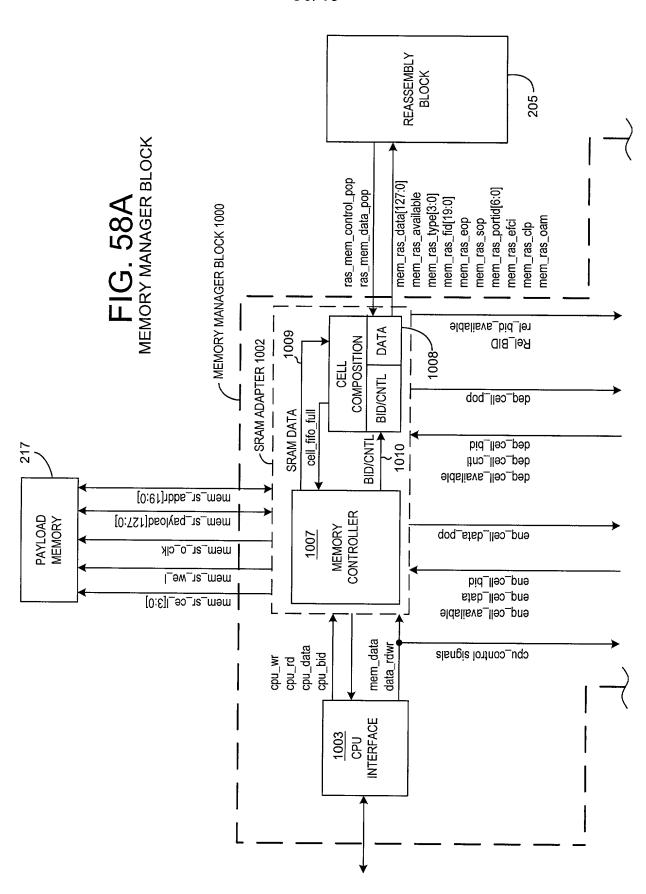
FIG. 56



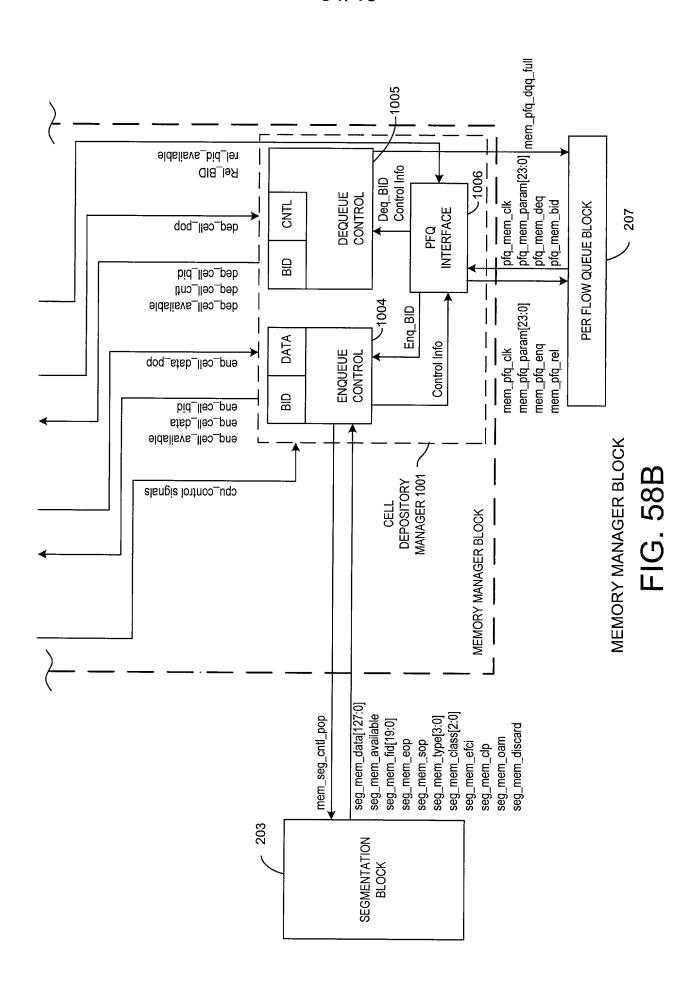




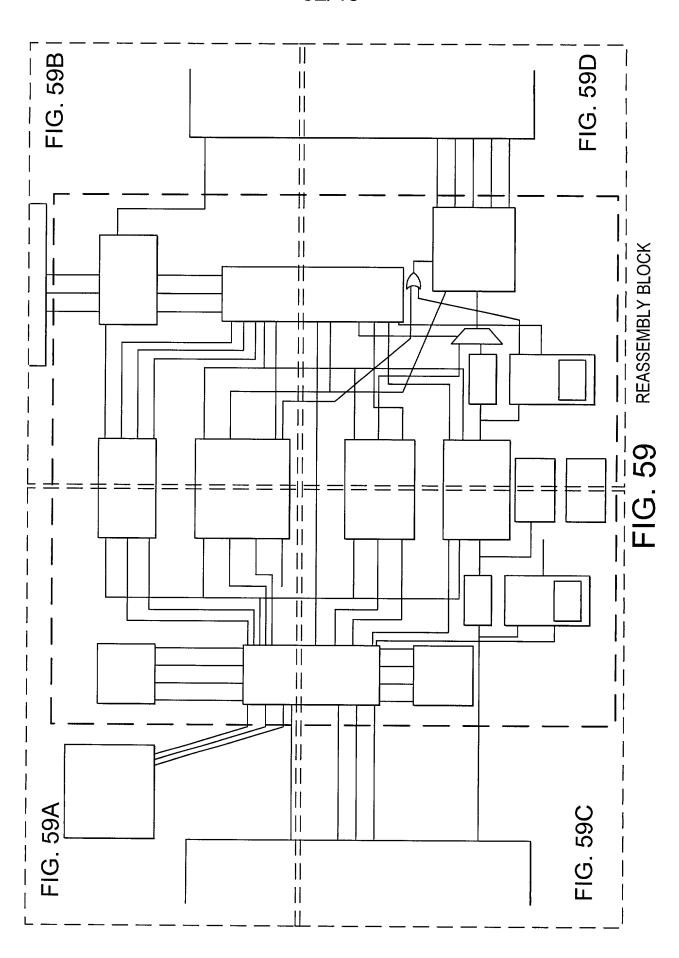


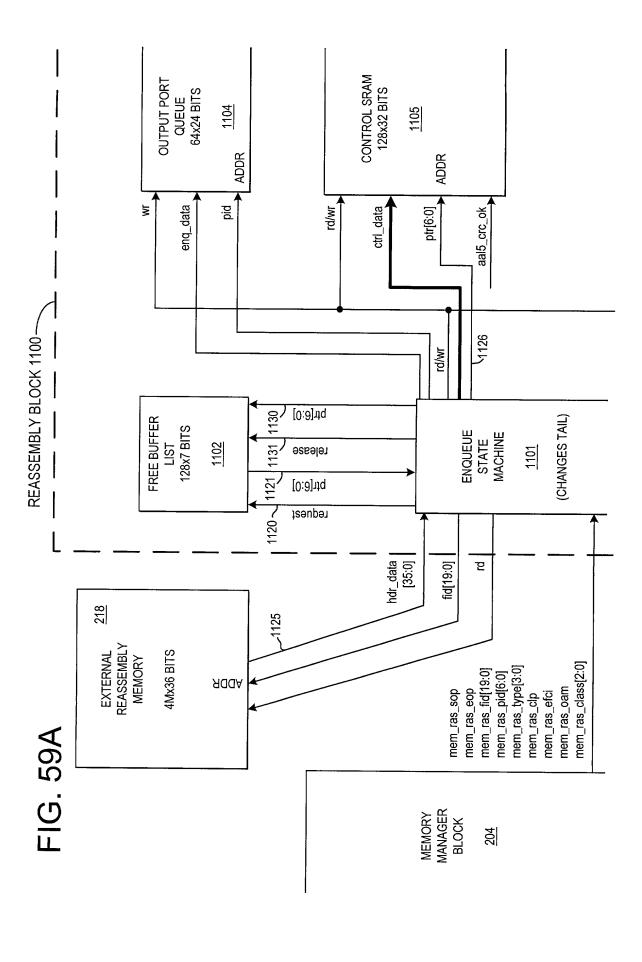


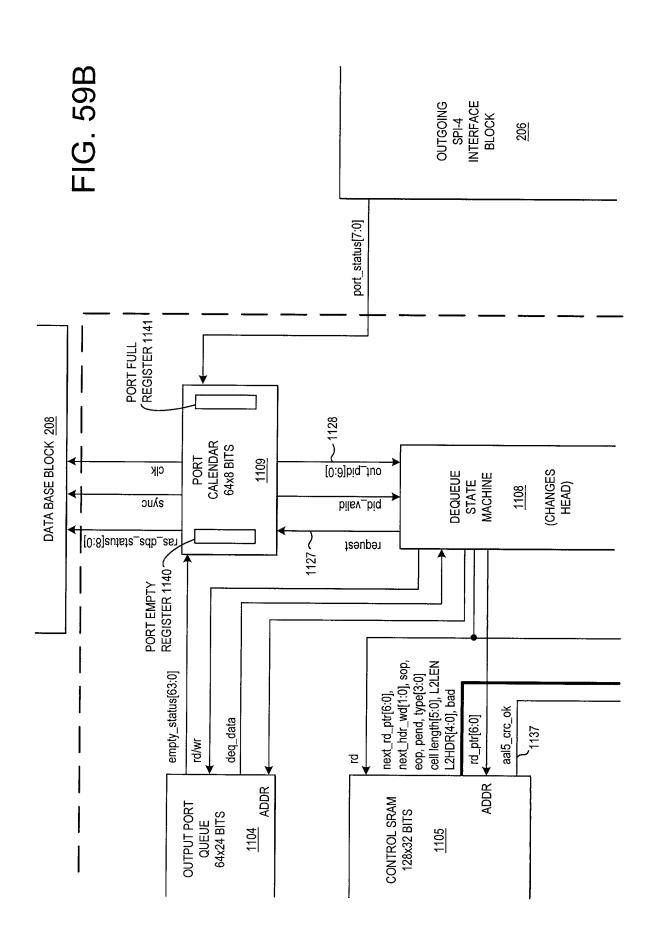




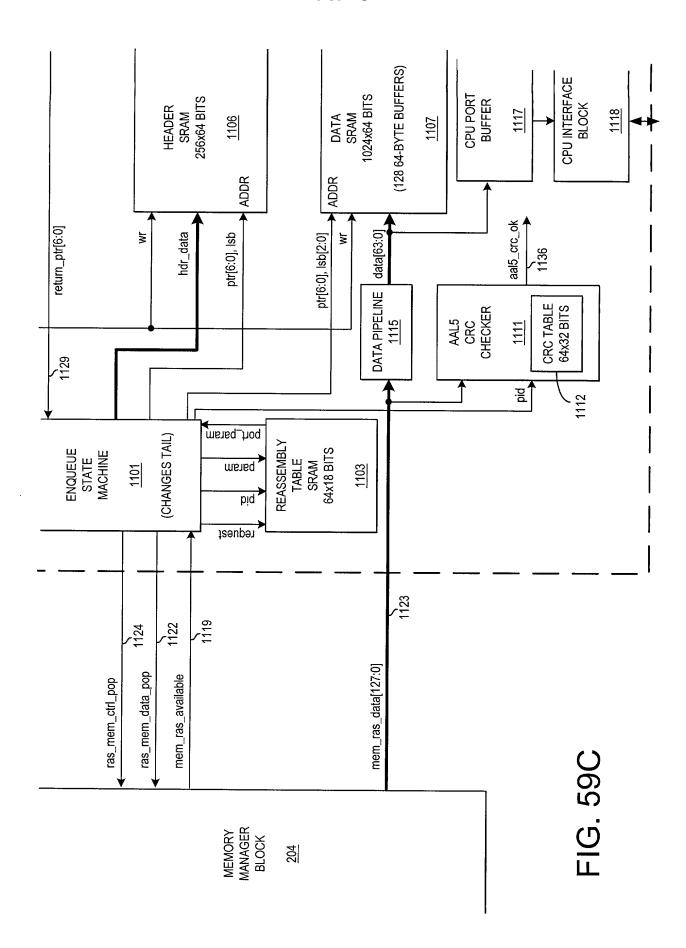




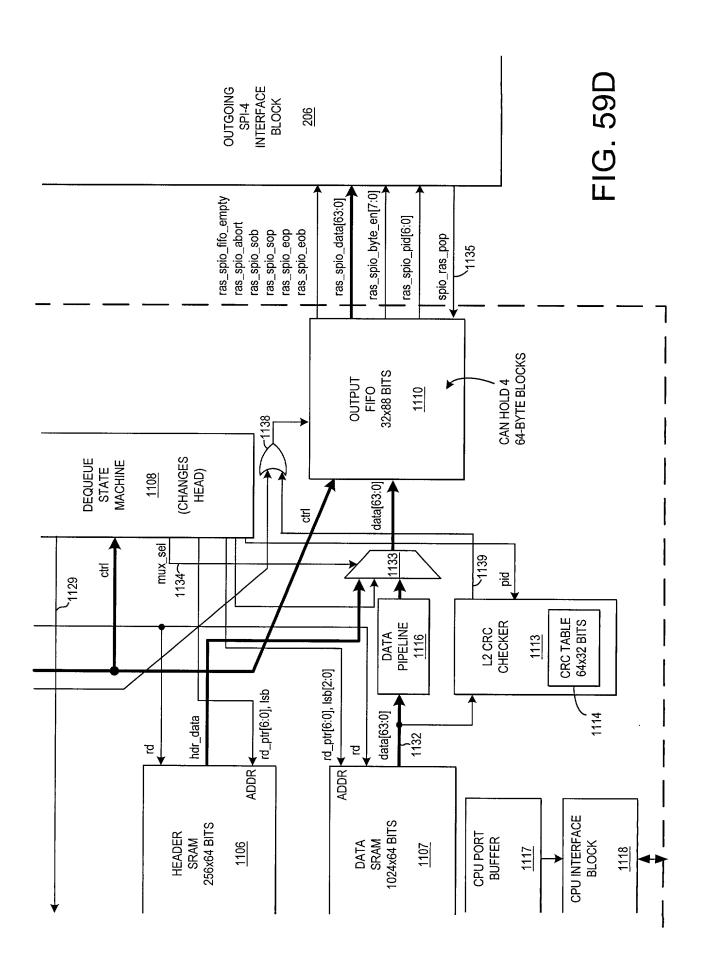


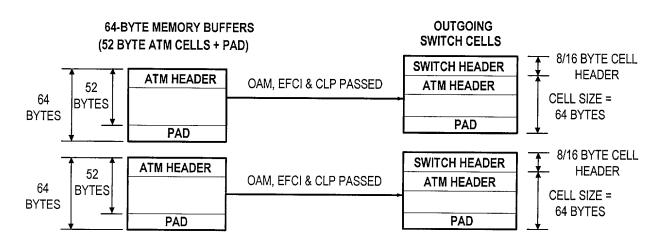












REASSEMBLY TYPE 1 (INGRESS APPLICATION TYPE 0)

FIG. 60A

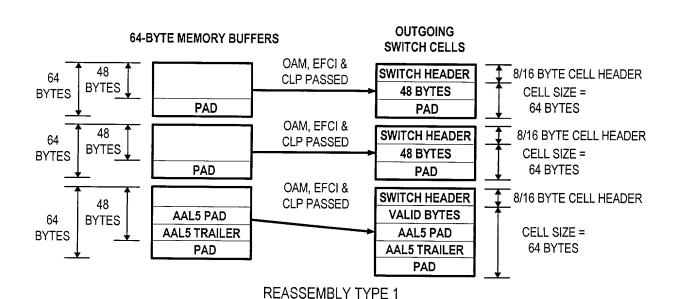
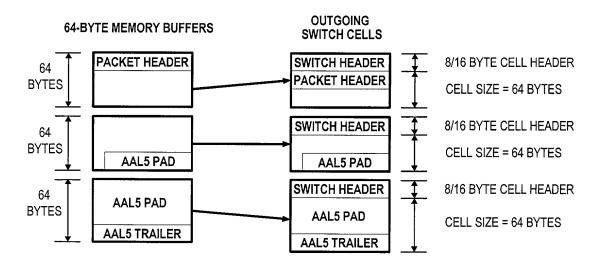


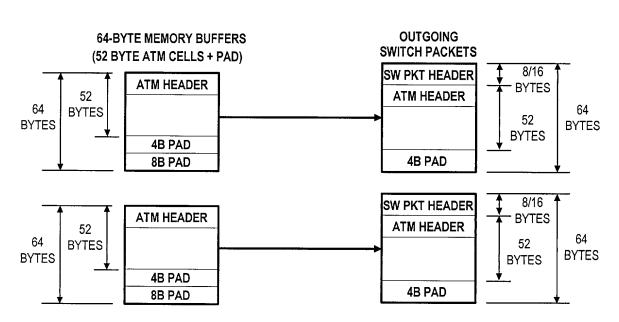
FIG. 60B

(INGRESS APPLICATION TYPE 1)



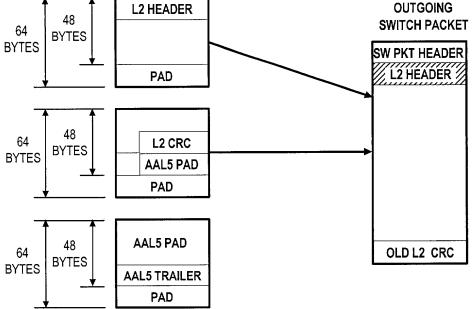
REASSEMBLY TYPE 1 (INGRESS APPLICATION TYPE 3)

FIG. 60C



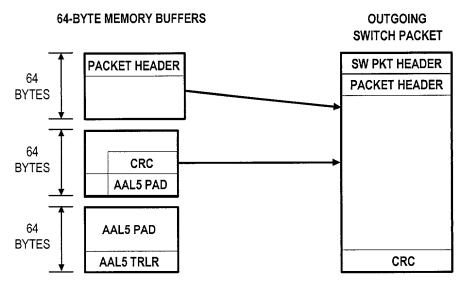
REASSEMBLY TYPE 2 (INGRESS APPLICATION TYPE 4) FIG. 60D

64-BYTE MEMORY BUFFERS (48 BYTE ATM CELLS + PAD) L2 HEADER



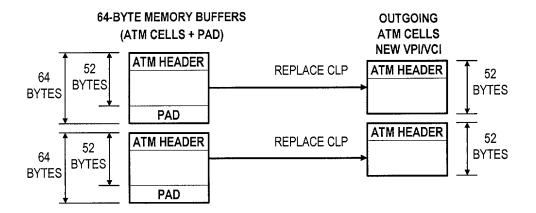
REASSEMBLY TYPE 3 (INGRESS APPLICATION TYPE 5)

FIG. 60E



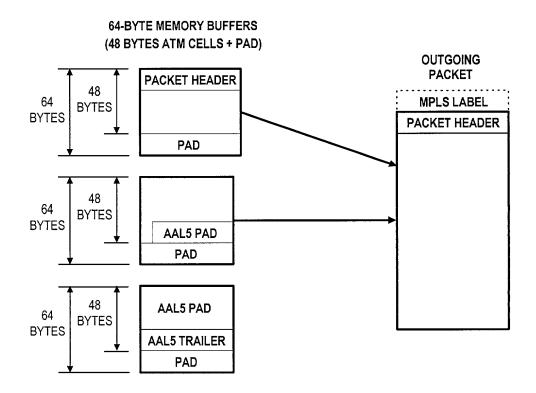
REASSEMBLY TYPE 4 (INGRESS APPLICATION TYPE 6)

FIG. 60F



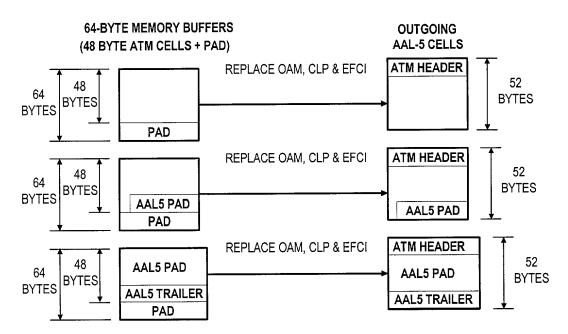
REASSEMBLY TYPE 5 (EGRESS APPLICATION TYPES 8 AND 12)

FIG. 60G



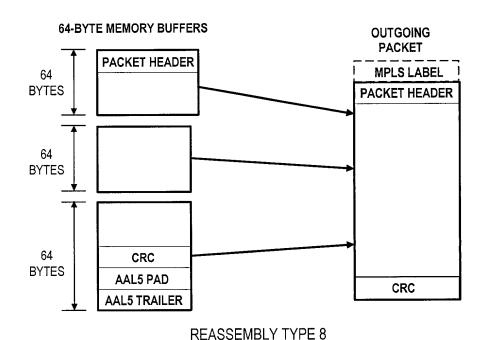
REASSEMBLY TYPE 6 (EGRESS APPLICATION TYPE 9)

FIG. 60H



REASSEMBLY TYPE 7 (INGRESS APPLICATION TYPES 10 AND 13)

FIG. 601



(INGRESS APPLICATION TYPES 11 AND 14) FIG. 60J

